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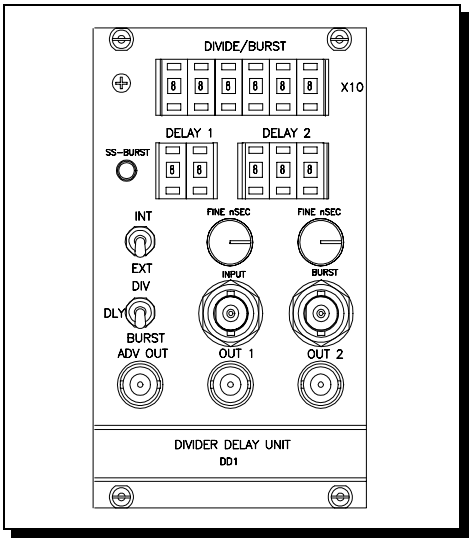
MODEL DD1
DIVIDER DELAY UNIT
DATA SHEET 734

MODEL DD1



DIVIDER DELAY PLUG-IN
FOR PULSE PICKER SYSTEMS

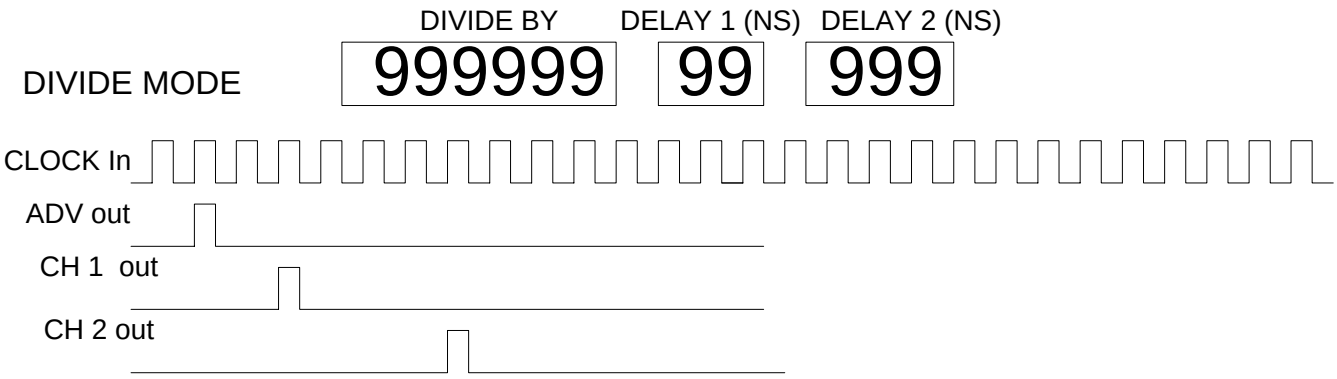
Model DD1 count down electronics is a high speed divider card capable of generating ***two*** independently delayable trigger pulses from a clock train input. (The clock may be an ext 1-250 MHz clock or the internal 250MHz clock). The output rate is set accurately by ***six*** decade thumb wheel switches while the delay is set by a ***two*** decade range. The mode-locker input is divided down an ECL divide by ***ten*** prescaler.

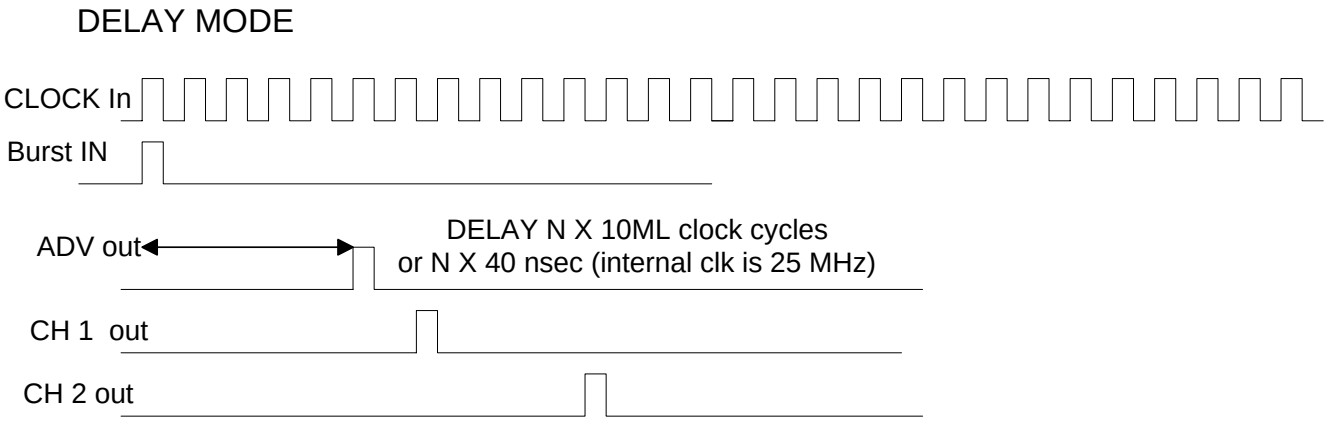
Model DD1 has ***three*** different modes of operation. The divide mode creates a continuous stream of pulses at a repetition rate equal to the clock frequency, divided by the digits on the preset switches. The ready mode allows the unit to be programmed as to a single shot or a burst of N pulses appearing once every ***ten*** clock cycles. The unit may be triggered by a manual burst switch or via an external burst input. It has ***two*** independently adjustable, high resolution precision delays. The standard range of these ***two*** delays is ***99 & 999*** nsec with an infinitely resolvable range of ***30*** nsec. For simple single pulse extraction**,** only output **1** is used. For double pulse applications as in regenerative amplifiers, one precisely delayed pulse is to carry out the injection seeding, the other pulse is used to extract the amplified pulse after a sufficient build up time. The ***two*** output delayed pulses may be also used to trigger ***two*** fast HV pulses (such as the **HVP-590-D or 525-D drivers**) from a differential Pockels cell switch out to create a fast optical gate. Typical jitter is less than 100 psec. On Delay and Burst Modes with Ext clock and arbritary trigger jitter is +/- ½ clock period.

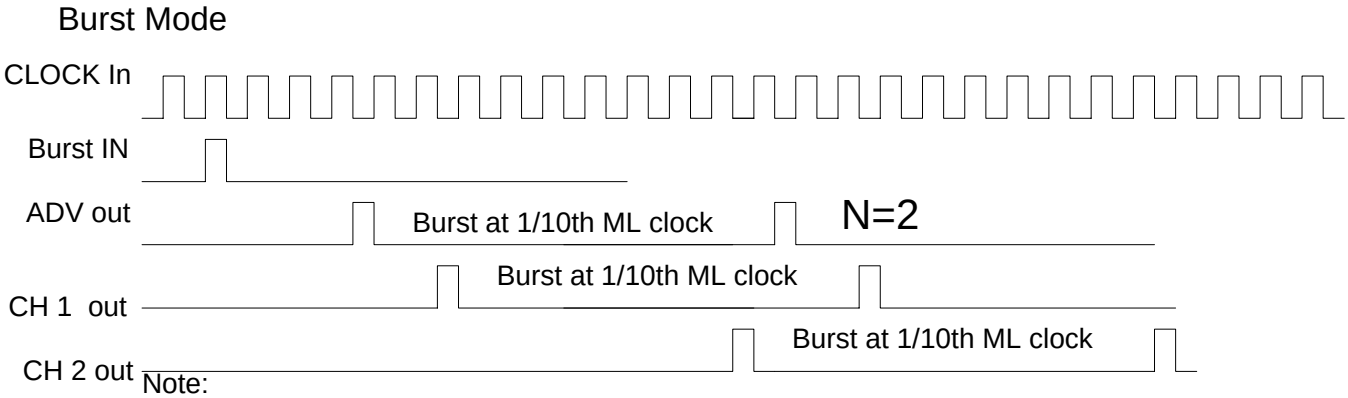
The advance output provides a convenient trigger pulse, absent from any programmed delay. The output trigger levels are three volts into 50 ohms. The **Model DD1** unit is compatible with all of Quantum Technology's " Pulse Picker " systems. (Please see Data Sheets 727, 732 and 739). This Plug-In may be purchased as part of a complete system with a " Pulse Picker ", or as a stand alone system in a small "S" Euro-Card cabinet with a power supply, or as a Plug-In module only for integration in other Quantum equipment. Other Delay options are available. (Please inquire).

SPECIFICATIONS:

Input Trigger Voltage	**TTL**
Clock Frequency EXT, INT	**200 MHz (to 1 MHz typical) 0.1-1vpp, 250 MHz int effective clock**
Output Rep Rate Range	**10 MHz to 10 Hz. (at 100 MHz clock)**
Delay Range (Delay 1)	**0-99 nsec (Digital), 30 nsec (Analog)**
Delay 2	**0-999 nsec (Digital), 30 nsec (Analog)**
Burst or single shot capability	**Manual or on command**
Output pulse levels into 50 ohms	**3 Volts., ADV, Out 1 & Out 2**
Output pulse widths (typical)	**50 nsec (Out 1), 50 nsec (Out 2)**
Size:	**3"x5"x8.5" Eurocard.**
Modes (where N = 999999x10)	**Divide Ext clock: ext clk ÷ N**
	Int clk: 250 MHz ÷ (Nx10)
	Range: F out = 1 MHz - 10Hz with ext. 100 MHz clk
Jitter:	**Int clk jitter +/- half clk, Ext clk +/- 200 psec**
	Delay: by N clk cycles
	Range: 30 nsec - 40 msec, 40 nsec/step int clk
	30nsec - 100 msec, 100 nsec/step ext clk
Jitter:	**Ext clk jitter +/- half clk, Int clk +/- 1nsec**
	Burst:
	1-999999 Burst @ frequency of CLK/10
	Ex: 2 = 2 pulses at 25 MHz (int clk) or 10 MHz (100 MHz Ext clk)
Jitter:	**Ext clk jitter +/- half clk, Int clk +/- 1nsec**







Note:
CLOCK In can be external 1-200MHz or or internal clock
If EXT ML clock is **not** phase synchronous with ext Burst/Gate IN
then Jitter on output is +/- 1/2 ML clock cycle

DD1 Unit Typical Timing