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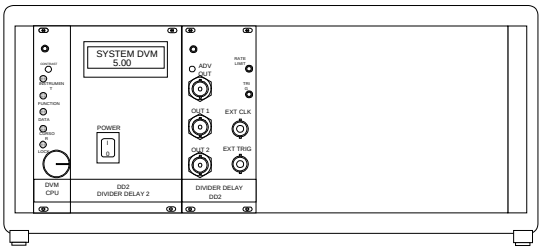
MODEL DD2

DIGITAL DIVIDER DELAY 2
DATA SHEET 773

DATA SHEET 773
MODEL DD2 –DIGITAL DIVIDER DELAY UNIT



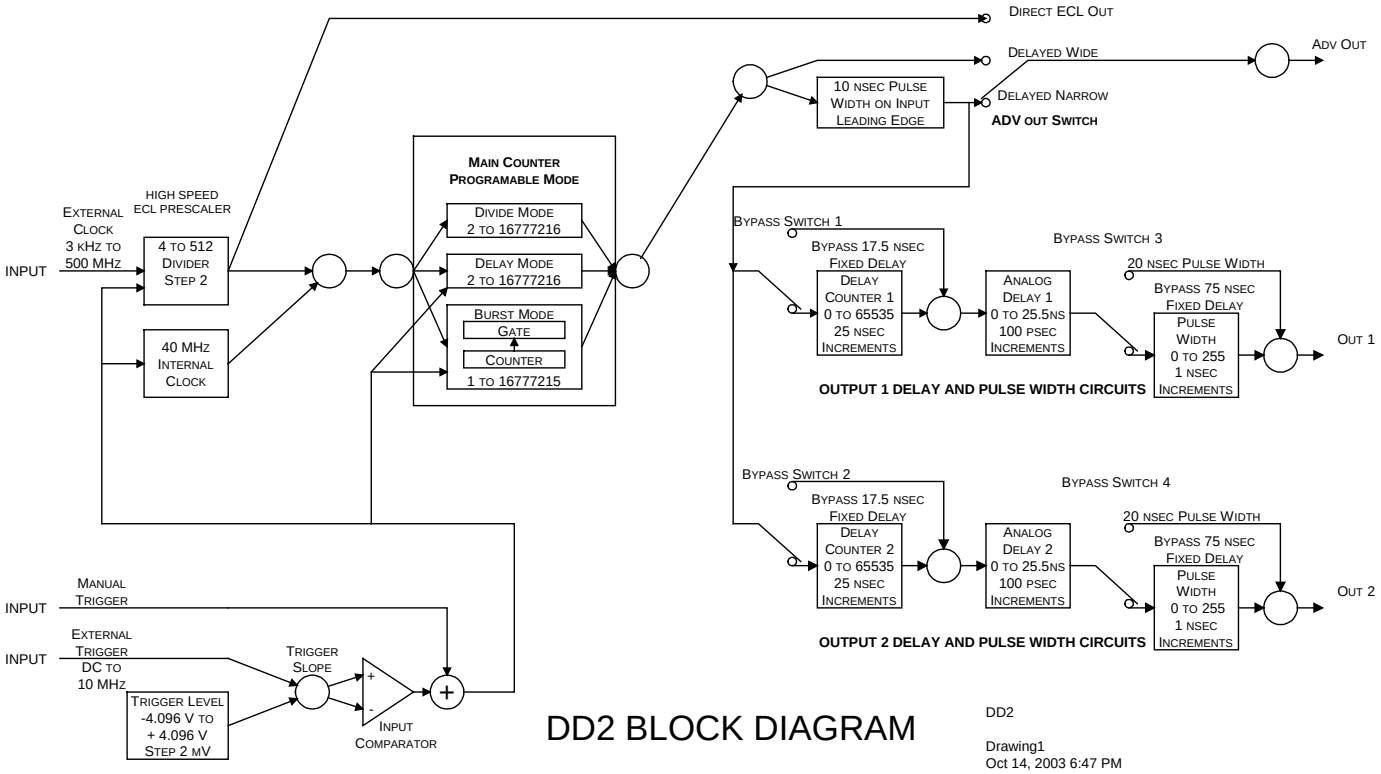
The Model DD2 is a modular divider/delay pulse generator designed to provide precise timing for electro-optic systems. It is a standard plug-in that conforms to the standard Quantum Technology chassis. It is powered by the chassis and controlled by the chassis control module.
Two output channels are available, each with:

Fine analog Delay:	0 to 25.5 nsec in 100 psec steps.
Digital Delay:	0 to 1.638 msec (65536 steps) in 25 nsec steps.
Pulse Width	1 to 255 nsec in 1.0 nsec steps.
Amplitude:	3.5 V pulse into 50 Ohms (Baseline is 0V).
rise time:	2 nsec
fall time:	4 nsec

Advanced Output Channel for synchronization of other equipment.
Internal (40 MHz) or External (3 kHz to >500 MHz) Clock.
External Trigger for Delay and Burst Modes. Very flexible input, accepts logic level or detector output (positive or negative envelope). - 4.096 V to + 4.096 V. DC to 200 MHz for signal components; External Trigger Repetition rate must be less than system repetition rate. Input power must be limited to .1 watt. Triggering on either positive or negative slope may be selected. Resolution is 2 mV. Accuracy below 3.3 V (absolute) is 10 mV. Above absolute 3.3 V, internal limiting of the signals degrades accuracy, but is useable.
Manual Trigger: Depressing the Manual Trigger Push Button enters a single external trigger pulse. The result is the same as a single pulse applied to the external trigger input.
System Mode: The main counter of the DD2 can be operated in 3 modes: Divide, Delay, and Burst. Different units are displayed in the Main Counter Data Mode to indicate the system mode in effect.
Divide mode divides the clock by the data entry (2-16777216). The unit is ratio. External trigger does not affect the signal in Divide mode. The main counter may be bypassed to obtain higher output pulse rate. With External Clock, further division of 4 to 512 in steps of 2 is available.
Delay mode delays the output by the data entry (2-16777216) number of clock cycles from the external trigger. The unit is count. Trigger level and trigger slopes determine trigger point on external trigger signal. This delay is from trigger in and affects the Advanced Output as well the two output channels.
Burst mode outputs the data entry (1-16777215) number of clock pulses starting at the external trigger. The unit is pulses. Trigger level and trigger slopes determine trigger point on external trigger signal. Output pulse rate will be determined by the division settings in divide mode and by the external trigger rate in delay and burst modes. A factory setting limits this rate to protect the subsequent drive circuits.

MODEL DD2 - DIVIDER DELAY 2 SPECIFICATIONS

Parameter	Value
Outputs	
Output Channels	Two (2) outputs, each with independent digitally controlled coarse delay, fine delay, and pulse width.
Coarse Delay Range per channel	1 to 65535 counts of 25 nsec (2.6214 ms) or Pre-scaled External Clock Period (6.1407 ms with 80MHz typ ext input)
Fine Delay Range per channel	0 to 25.5 nsec, 100 psec resolution
Pulse Width Range per channel	1 to 255 nsec, 1 nsec resolution
Output Rise Time (50 Ohms)	2 nsec
Output Fall Time (50 Ohms)	4 nsec
Modes	Divide, Delay, Burst, Main Counter Bypassed
Divide Range	2 to 16777216 (Ratio) (Divide Pulse Rate of Internal Clock or Prescaled External Clock, with 80 MHz typ external clock & prescale @4, max output rate is 20MHz with in divide bypass mode)
Delay Range	2 to 16777216 (Counts) (Number of Pulses at Internal Clock (67.09 ms) or Prescaled External Clock Delay to Output)
Burst Range	1 to 16777215 (Pulses) (Number of Output Pulses at Internal Clock or Prescaled External Clock)
	***With 40MHz Internal Clock Rate Generator**
Adv Out Modes	Direct Pre-scale Out, Delayed Wide, Delayed Narrow
Pulse Width—Internal Clock	7 nsec, 12 nsec
Pulse Width—External Clock	7 nsec, Prescaled Pulse Width
Delay from External Trigger	114 nsec (2 Counts Delay is Minimum)
External Trigger Type	Level Crossing at Selected Slope (+ or -)
Level (typ input, may be TTL or Photodiode)	-4096 to 4096 mV in 2 mV Steps
External Clock	
Frequency Range	3 kHz to >500MHz
Prescaler Division Range	4 to 512 in Steps of 2
General	
Internal Non-Volatile Storage	8 Configurations (Including Power up of Last State)



DD2 BLOCK DIAGRAM

DD2

Drawing1
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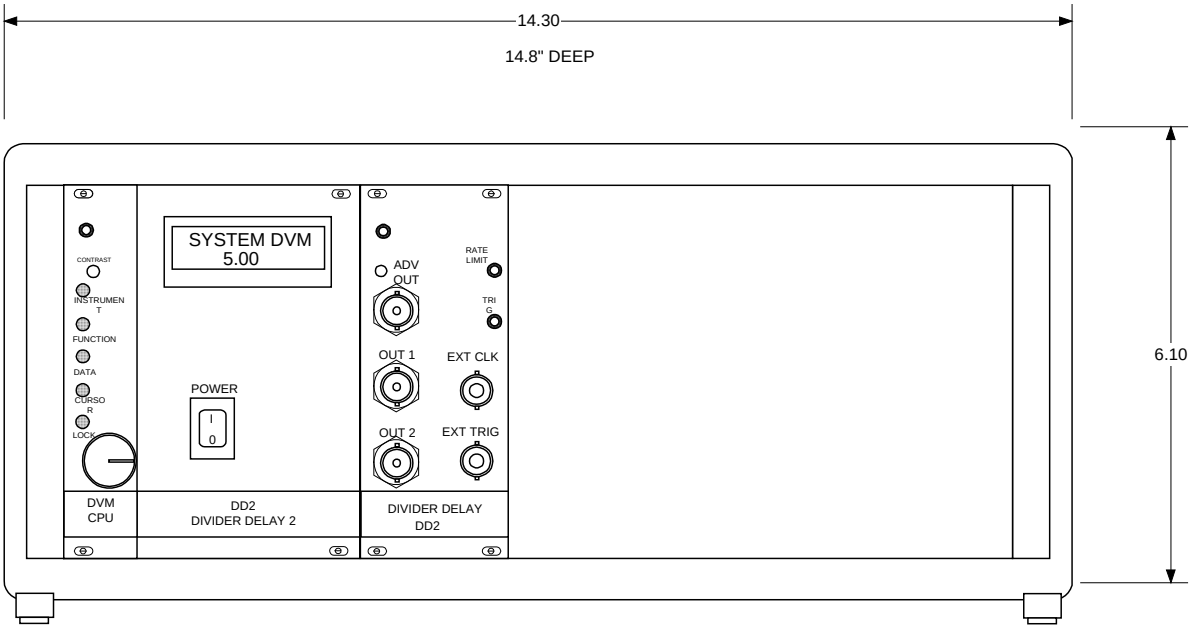

DD2 STAND ALONE CABINET